<stdout>: Warning (graph_child_address): /vop@ff370000/port: graph node has single child node 'endpoint@0', #address-cells/#size-cells are not necessary
/dts-v1/;

/ {
	compatible = "azw,beelink-a1\0rockchip,rk3328";
	interrupt-parent = <0x01>;
	#address-cells = <0x02>;
	#size-cells = <0x02>;
	model = "Beelink A1";

	aliases {
		serial0 = "/serial@ff110000";
		serial1 = "/serial@ff120000";
		serial2 = "/serial@ff130000";
		i2c0 = "/i2c@ff150000";
		i2c1 = "/i2c@ff160000";
		i2c2 = "/i2c@ff170000";
		i2c3 = "/i2c@ff180000";
		ethernet0 = "/ethernet@ff540000";
		ethernet1 = "/ethernet@ff550000";
		mmc0 = "/mmc@ff500000";
		mmc1 = "/mmc@ff520000";
	};

	cpus {
		#address-cells = <0x02>;
		#size-cells = <0x00>;

		cpu@0 {
			device_type = "cpu";
			compatible = "arm,cortex-a53";
			reg = <0x00 0x00>;
			clocks = <0x02 0x06>;
			#cooling-cells = <0x02>;
			cpu-idle-states = <0x03>;
			dynamic-power-coefficient = <0x78>;
			enable-method = "psci";
			next-level-cache = <0x04>;
			operating-points-v2 = <0x05>;
			cpu-supply = <0x06>;
			phandle = <0x09>;
		};

		cpu@1 {
			device_type = "cpu";
			compatible = "arm,cortex-a53";
			reg = <0x00 0x01>;
			clocks = <0x02 0x06>;
			#cooling-cells = <0x02>;
			cpu-idle-states = <0x03>;
			dynamic-power-coefficient = <0x78>;

```
        enable-method = "psci";
        next-level-cache = <0x04>;
        operating-points-v2 = <0x05>;
        cpu-supply = <0x06>;
        phandle = <0x0a>;
};

cpu@2 {
        device_type = "cpu";
        compatible = "arm,cortex-a53";
        reg = <0x00 0x02>;
        clocks = <0x02 0x06>;
        #cooling-cells = <0x02>;
        cpu-idle-states = <0x03>;
        dynamic-power-coefficient = <0x78>;
        enable-method = "psci";
        next-level-cache = <0x04>;
        operating-points-v2 = <0x05>;
        cpu-supply = <0x06>;
        phandle = <0x0b>;
};

cpu@3 {
        device_type = "cpu";
        compatible = "arm,cortex-a53";
        reg = <0x00 0x03>;
        clocks = <0x02 0x06>;
        #cooling-cells = <0x02>;
        cpu-idle-states = <0x03>;
        dynamic-power-coefficient = <0x78>;
        enable-method = "psci";
        next-level-cache = <0x04>;
        operating-points-v2 = <0x05>;
        cpu-supply = <0x06>;
        phandle = <0x0c>;
};

idle-states {
        entry-method = "psci";

        cpu-sleep {
                compatible = "arm,idle-state";
                local-timer-stop;
                arm,psci-suspend-param = <0x10000>;
                entry-latency-us = <0x78>;
                exit-latency-us = <0xfa>;
                min-residency-us = <0x384>;
                phandle = <0x03>;
        };
};

l2-cache0 {
```

```
                compatible = "cache";
                phandle = <0x04>;
        };
};

        opp-table-0 table0 {
                compatible = "operating-points-v2";
                opp-shared;
                phandle = <0x05>;

                opp-408000000 {
                        opp-hz = <0x00 0x18519600>;
                        opp-microvolt = <0xe7ef0>;
                        clock-latency-ns = <0x9c40>;
                        opp-suspend;
                };

                opp-600000000 {
                        opp-hz = <0x00 0x23c34600>;
                        opp-microvolt = <0xe7ef0>;
                        clock-latency-ns = <0x9c40>;
                };

                opp-816000000 {
                        opp-hz = <0x00 0x30a32c00>;
                        opp-microvolt = <0xf4240>;
                        clock-latency-ns = <0x9c40>;
                };

                opp-1008000000 {
                        opp-hz = <0x00 0x3c14dc00>;
                        opp-microvolt = <0x10c8e0>;
                        clock-latency-ns = <0x9c40>;
                };

                opp-1200000000 {
                        opp-hz = <0x00 0x47868c00>;
                        opp-microvolt = <0x12b128>;
                        clock-latency-ns = <0x9c40>;
                };

                opp-1296000000 {
                        opp-hz = <0x00 0x4d3f6400>;
                        opp-microvolt = <0x13d620>;
                        clock-latency-ns = <0x9c40>;
                };
        };

        bus {
                compatible = "simple-bus";
                #address-cells = <0x02>;
                #size-cells = <0x02>;
```

```
                ranges;
                phandle = <0x72>;

                dmac@ff1f0000 {
                        compatible = "arm,pl330\0arm,primecell";
                        reg = <0x00 0xff1f0000 0x00 0x4000>;
                        interrupts = <0x00 0x00 0x04 0x00 0x01 0x04>;
                        arm,pl330-periph-burst;
                        clocks = <0x02 0x86>;
                        clock-names = "apb_pclk";
                        #dma-cells = <0x01>;
                        phandle = <0x10>;
                };
        };

        analog-sound {
                compatible = "simple-audio-card";
                simple-audio-card,format = "i2s";
                simple-audio-card,mclk-fs = <0x100>;
                simple-audio-card,name = "Analog A/V";
                status = "okay";
                phandle = <0x720x73>;

                simple-audio-card,cpu {
                        sound-dai = <0x07>;
                };

                simple-audio-card,codec {
                        sound-dai = <0x08>;
                };
        };

        arm-pmu {
                compatible = "arm,cortex-a53-pmu";
                interrupts = <0x00 0x64 0x04 0x00 0x65 0x04 0x00 0x66 0x04 0x00 0x67 0x04>;
                interrupt-affinity = <0x09 0x0a 0x0b 0x0c>;
        };

        display-subsystem {
                compatible = "rockchip,display-subsystem";
                ports = <0x0d>;
                phandle = <0x730x74>;
        };

        hdmi-sound {
                compatible = "simple-audio-card";
                simple-audio-card,format = "i2s";
                simple-audio-card,mclk-fs = <0x80>;
                simple-audio-card,name = "HDMI";
                status = "okay";
                phandle = <0x740x75>;
```

```
                simple-audio-card,cpu {
                        sound-dai = <0x0e>;
                };

                simple-audio-card,codec {
                        sound-dai = <0x0f>;
                };
        };

        psci {
                compatible = "arm,psci-1.0\0arm,psci-0.2";
                method = "smc";
        };

        timer {
                compatible = "arm,armv8-timer";
                interrupts = <0x01 0x0d 0xf08 0x01 0x0e 0xf08 0x01 0x0b 0xf08 0x01 0x0a
0xf08>;
        };

        xin24m {
                compatible = "fixed-clock";
                #clock-cells = <0x00>;
                clock-frequency = <0x16e3600>;
                clock-output-names = "xin24m";
                phandle = <0x49>;
        };

        i2s@ff000000 {
                compatible = "rockchip,rk3328-i2s\0rockchip,rk3066-i2s";
                reg = <0x00 0xff000000 0x00 0x1000>;
                interrupts = <0x00 0x1a 0x04>;
                clocks = <0x02 0x29 0x02 0x137>;
                clock-names = "i2s_clk\0i2s_hclk";
                dmas = <0x10 0x0b 0x10 0x0c>;
                dma-names = "tx\0rx";
                #sound-dai-cells = <0x00>;
                status = "okay";
                phandle = <0x0e>;
        };

        i2s@ff010000 {
                compatible = "rockchip,rk3328-i2s\0rockchip,rk3066-i2s";
                reg = <0x00 0xff010000 0x00 0x1000>;
                interrupts = <0x00 0x1b 0x04>;
                clocks = <0x02 0x2a 0x02 0x138>;
                clock-names = "i2s_clk\0i2s_hclk";
                dmas = <0x10 0x0e 0x10 0x0f>;
                dma-names = "tx\0rx";
                #sound-dai-cells = <0x00>;
                status = "okay";
                phandle = <0x07>;
```

```
};

i2s@ff020000 {
	compatible = "rockchip,rk3328-i2s\0rockchip,rk3066-i2s";
	reg = <0x00 0xff020000 0x00 0x1000>;
	interrupts = <0x00 0x1c 0x04>;
	clocks = <0x02 0x2b 0x02 0x139>;
	clock-names = "i2s_clk\0i2s_hclk";
	dmas = <0x10 0x00 0x10 0x01>;
	dma-names = "tx\0rx";
	#sound-dai-cells = <0x00>;
	status = "disabled";
	phandle = <0x750x76>;
};

spdif@ff030000 {
	compatible = "rockchip,rk3328-spdif";
	reg = <0x00 0xff030000 0x00 0x1000>;
	interrupts = <0x00 0x1d 0x04>;
	clocks = <0x02 0x2e 0x02 0x13a>;
	clock-names = "mclk\0hclk";
	dmas = <0x10 0x0a>;
	dma-names = "tx";
	pinctrl-names = "default";
	pinctrl-0 = <0x11>;
	#sound-dai-cells = <0x00>;
	status = "okay";
	phandle = <0x70>;
};

pdm@ff040000 {
	compatible = "rockchip,pdm";
	reg = <0x00 0xff040000 0x00 0x1000>;
	clocks = <0x02 0x3d 0x02 0x152>;
	clock-names = "pdm_clk\0pdm_hclk";
	dmas = <0x10 0x10>;
	dma-names = "rx";
	pinctrl-names = "default\0sleep";
	pinctrl-0 = <0x12 0x13 0x14 0x15 0x16>;
	pinctrl-1 = <0x17 0x18 0x19 0x1a 0x1b>;
	status = "disabled";
	phandle = <0x760x77>;
};

syscon@ff100000 {
	compatible = "rockchip,rk3328-grf\0syscon\0simple-mfd";
	reg = <0x00 0xff100000 0x00 0x1000>;
	phandle = <0x3a>;

	io-domains {
		compatible = "rockchip,rk3328-io-voltage-domain";
		status = "okay";
```

```
                vccio1-supply = <0x1c>;
                vccio2-supply = <0x1d>;
                vccio3-supply = <0x1c>;
                vccio4-supply = <0x1e>;
                vccio5-supply = <0x1c>;
                vccio6-supply = <0x1e>;
                pmuio-supply = <0x1c>;
                phandle = <0x770x78>;
        };

        grf-gpio {
                compatible = "rockchip,rk3328-grf-gpio";
                gpio-controller;
                #gpio-cells = <0x02>;
                phandle = <0x48>;
        };

        power-controller {
                compatible = "rockchip,rk3328-power-controller";
                #power-domain-cells = <0x01>;
                #address-cells = <0x01>;
                #size-cells = <0x00>;
                phandle = <0x3c>;

                power-domain@1 {
                        reg = <0x01>;
                        clocks = <0x02 0x87>;
                        #power-domain-cells = <0x00>;
                };

                power-domain@6 {
                        reg = <0x06>;
                        #power-domain-cells = <0x00>;
                };

                power-domain@5 {
                        reg = <0x05>;
                        clocks = <0x02 0x8b 0x02 0x142 0x02 0x41 0x02 0x42>;
                        #power-domain-cells = <0x00>;
                };

                power-domain@8 {
                        reg = <0x08>;
                        clocks = <0x02 0x8f 0x02 0x146>;
                        #power-domain-cells = <0x00>;
                };
        };

        reboot-mode {
                compatible = "syscon-reboot-mode";
                offset = <0x5c8>;
                mode-normal = <0x5242c300>;
```

```
                mode-recovery = <0x5242c303>;
                mode-bootloader = <0x5242c309>;
                mode-loader = <0x5242c301>;
        };
};

serial@ff110000 {
        compatible = "rockchip,rk3328-uart\0snps,dw-apb-uart";
        reg = <0x00 0xff110000 0x00 0x100>;
        interrupts = <0x00 0x37 0x04>;
        clocks = <0x02 0x26 0x02 0xd2>;
        clock-names = "baudclk\0apb_pclk";
        dmas = <0x10 0x02 0x10 0x03>;
        dma-names = "tx\0rx";
        pinctrl-names = "default";
        pinctrl-0 = <0x1f 0x20 0x21>;
        reg-io-width = <0x04>;
        reg-shift = <0x02>;
        status = "disabled";
        phandle = <0x780x79>;
};

serial@ff120000 {
        compatible = "rockchip,rk3328-uart\0snps,dw-apb-uart";
        reg = <0x00 0xff120000 0x00 0x100>;
        interrupts = <0x00 0x38 0x04>;
        clocks = <0x02 0x27 0x02 0xd3>;
        clock-names = "baudclk\0apb_pclk";
        dmas = <0x10 0x04 0x10 0x05>;
        dma-names = "tx\0rx";
        pinctrl-names = "default";
        pinctrl-0 = <0x22 0x23 0x24>;
        reg-io-width = <0x04>;
        reg-shift = <0x02>;
        status = "disabled";
        phandle = <0x790x7a>;
};

serial@ff130000 {
        compatible = "rockchip,rk3328-uart\0snps,dw-apb-uart";
        reg = <0x00 0xff130000 0x00 0x100>;
        interrupts = <0x00 0x39 0x04>;
        clocks = <0x02 0x28 0x02 0xd4>;
        clock-names = "baudclk\0apb_pclk";
        dmas = <0x10 0x06 0x10 0x07>;
        dma-names = "tx\0rx";
        pinctrl-names = "default";
        pinctrl-0 = <0x25>;
        reg-io-width = <0x04>;
        reg-shift = <0x02>;
        status = "okay";
        phandle = <0x7a0x7b>;
```

```
};

i2c@ff150000 {
	compatible = "rockchip,rk3328-i2c\0rockchip,rk3399-i2c";
	reg = <0x00 0xff150000 0x00 0x1000>;
	interrupts = <0x00 0x24 0x04>;
	#address-cells = <0x01>;
	#size-cells = <0x00>;
	clocks = <0x02 0x37 0x02 0xcd>;
	clock-names = "i2c\0pclk";
	pinctrl-names = "default";
	pinctrl-0 = <0x26>;
	status = "disabled";
	phandle = <0x7b0x7e>;
};

i2c@ff160000 {
	compatible = "rockchip,rk3328-i2c\0rockchip,rk3399-i2c";
	reg = <0x00 0xff160000 0x00 0x1000>;
	interrupts = <0x00 0x25 0x04>;
	#address-cells = <0x01>;
	#size-cells = <0x00>;
	clocks = <0x02 0x38 0x02 0xce>;
	clock-names = "i2c\0pclk";
	pinctrl-names = "default";
	pinctrl-0 = <0x27>;
	status = "okay";
	clock-frequency = <0xf4240>;
	i2c-scl-falling-time-ns = <0x05>;
	i2c-scl-rising-time-ns = <0x53>;
	phandle = <0x7c0x7d>;

	pmic@18 {
		compatible = "rockchip,rk805";
		reg = <0x18>;
		interrupt-parent = <0x28>;
		interrupts = <0x06 0x08>;
		pinctrl-names = "default";
		pinctrl-0 = <0x29>;
		rockchip,system-power-controller;
		wakeup-source;
		#clock-cells = <0x00>;
		vcc1-supply = <0x2a>;
		vcc2-supply = <0x2a>;
		vcc3-supply = <0x2a>;
		vcc4-supply = <0x2a>;
		vcc5-supply = <0x1c>;
		vcc6-supply = <0x1c>;

		regulators {

			DCDC_REG1 {
```

```
                regulator-name = "vdd_logic";
                regulator-min-microvolt = <0xaae60>;
                regulator-max-microvolt = <0x149970>;
                regulator-always-on;
                regulator-boot-on;
                phandle = <0x3d>;

                regulator-state-mem {
                        regulator-on-in-suspend;
                        regulator-suspend-microvolt = <0xf4240>;
                };
        };

        DCDC_REG2 {
                regulator-name = "vdd_arm";
                regulator-min-microvolt = <0xaae60>;
                regulator-max-microvolt = <0x149970>;
                regulator-always-on;
                regulator-boot-on;
                phandle = <0x06>;

                regulator-state-mem {
                        regulator-on-in-suspend;
                        regulator-suspend-microvolt = <0xe7ef0>;
                };
        };

        DCDC_REG3 {
                regulator-name = "vcc_ddr";
                regulator-always-on;
                regulator-boot-on;
                phandle = <0x7d0x7e>;

                regulator-state-mem {
                        regulator-on-in-suspend;
                };
        };

        DCDC_REG4 {
                regulator-name = "vcc_io";
                regulator-min-microvolt = <0x325aa0>;
                regulator-max-microvolt = <0x325aa0>;
                regulator-always-on;
                regulator-boot-on;
                phandle = <0x1c>;

                regulator-state-mem {
                        regulator-on-in-suspend;
                        regulator-suspend-microvolt = <0x325aa0>;
                };
        };
```

```
                        LDO_REG1 {
                                regulator-name = "vdd_18";
                                regulator-min-microvolt = <0x1b7740>;
                                regulator-max-microvolt = <0x1b7740>;
                                regulator-always-on;
                                regulator-boot-on;
                                phandle = <0x1e>;

                                regulator-state-mem {
                                        regulator-on-in-suspend;
                                        regulator-suspend-microvolt = <0x1b7740>;
                                };
                        };

                        LDO_REG2 {
                                regulator-name = "vcc_18emmc";
                                regulator-min-microvolt = <0x1b7740>;
                                regulator-max-microvolt = <0x1b7740>;
                                regulator-always-on;
                                regulator-boot-on;
                                phandle = <0x1d>;

                                regulator-state-mem {
                                        regulator-on-in-suspend;
                                        regulator-suspend-microvolt = <0x1b7740>;
                                };
                        };

                        LDO_REG3 {
                                regulator-name = "vdd_11";
                                regulator-min-microvolt = <0x10c8e0>;
                                regulator-max-microvolt = <0x10c8e0>;
                                regulator-always-on;
                                regulator-boot-on;
                                phandle = <0x7e0x7f>;

                                regulator-state-mem {
                                        regulator-on-in-suspend;
                                        regulator-suspend-microvolt = <0x10c8e0>;
                                };
                        };
                };
        };
};

i2c@ff170000 {
        compatible = "rockchip,rk3328-i2c\0rockchip,rk3399-i2c";
        reg = <0x00 0xff170000 0x00 0x1000>;
        interrupts = <0x00 0x26 0x04>;
        #address-cells = <0x01>;
        #size-cells = <0x00>;
        clocks = <0x02 0x39 0x02 0xcf>;
```

```
		clock-names = "i2c\0pclk";
		pinctrl-names = "default";
		pinctrl-0 = <0x2b>;
		status = "disabled";
		phandle = <0x7f0x80>;
	};

	i2c@ff180000 {
		compatible = "rockchip,rk3328-i2c\0rockchip,rk3399-i2c";
		reg = <0x00 0xff180000 0x00 0x1000>;
		interrupts = <0x00 0x27 0x04>;
		#address-cells = <0x01>;
		#size-cells = <0x00>;
		clocks = <0x02 0x3a 0x02 0xd0>;
		clock-names = "i2c\0pclk";
		pinctrl-names = "default";
		pinctrl-0 = <0x2c>;
		status = "disabled";
		phandle = <0x800x81>;
	};

	spi@ff190000 {
		compatible = "rockchip,rk3328-spi\0rockchip,rk3066-spi";
		reg = <0x00 0xff190000 0x00 0x1000>;
		interrupts = <0x00 0x31 0x04>;
		#address-cells = <0x01>;
		#size-cells = <0x00>;
		clocks = <0x02 0x20 0x02 0xd1>;
		clock-names = "spiclk\0apb_pclk";
		dmas = <0x10 0x08 0x10 0x09>;
		dma-names = "tx\0rx";
		pinctrl-names = "default";
		pinctrl-0 = <0x2d 0x2e 0x2f 0x30>;
		status = "disabled";
		phandle = <0x810x82>;
	};

	watchdog@ff1a0000 {
		compatible = "rockchip,rk3328-wdt\0snpssnps,dw-wdt";
		reg = <0x00 0xff1a0000 0x00 0x100>;
		interrupts = <0x00 0x28 0x04>;
		clocks = <0x02 0xec>;
		phandle = <0x820x83>;
	};

	pwm@ff1b0000 {
		compatible = "rockchip,rk3328-pwm";
		reg = <0x00 0xff1b0000 0x00 0x10>;
		clocks = <0x02 0x3c 0x02 0xd6>;
		clock-names = "pwm\0pclk";
		pinctrl-names = "default";
		pinctrl-0 = <0x31>;
```

```
		#pwm-cells = <0x03>;
		status = "disabled";
		phandle = <0x830x84>;
	};

	pwm@ff1b0010 {
		compatible = "rockchip,rk3328-pwm";
		reg = <0x00 0xff1b0010 0x00 0x10>;
		clocks = <0x02 0x3c 0x02 0xd6>;
		clock-names = "pwm\0pclk";
		pinctrl-names = "default";
		pinctrl-0 = <0x32>;
		#pwm-cells = <0x03>;
		status = "disabled";
		phandle = <0x840x85>;
	};

	pwm@ff1b0020 {
		compatible = "rockchip,rk3328-pwm";
		reg = <0x00 0xff1b0020 0x00 0x10>;
		clocks = <0x02 0x3c 0x02 0xd6>;
		clock-names = "pwm\0pclk";
		pinctrl-names = "default";
		pinctrl-0 = <0x33>;
		#pwm-cells = <0x03>;
		status = "disabled";
		phandle = <0x850x86>;
	};

	pwm@ff1b0030 {
		compatible = "rockchip,rk3328-pwm";
		reg = <0x00 0xff1b0030 0x00 0x10>;
		interrupts = <0x00 0x32 0x04>;
		clocks = <0x02 0x3c 0x02 0xd6>;
		clock-names = "pwm\0pclk";
		pinctrl-names = "default";
		pinctrl-0 = <0x34>;
		#pwm-cells = <0x03>;
		status = "disabled";
		phandle = <0x860x87>;
	};

	dma-controller@ff1f0000 {
		compatible = "arm,pl330\0arm,primecell";
		reg = <0x00 0xff1f0000 0x00 0x4000>;
		interrupts = <0x00 0x00 0x04 0x00 0x01 0x04>;
		arm,pl330-periph-burst;
		clocks = <0x02 0x86>;
		clock-names = "apb_pclk";
		#dma-cells = <0x01>;
		phandle = <0x10>;
	};
```

```
        thermal-zones {

                soc-thermal {
                        polling-delay-passive = <0x14>;
                        polling-delay = <0x3e8>;
                        sustainable-power = <0x3e8>;
                        thermal-sensors = <0x35 0x00>;
                        phandle = <0x870x88>;

                        trips {

                                trip-point0 {
                                        temperature = <0x11170>;
                                        hysteresis = <0x7d0>;
                                        type = "passive";
                                        phandle = <0x880x89>;
                                };

                                trip-point1 {
                                        temperature = <0x14c08>;
                                        hysteresis = <0x7d0>;
                                        type = "passive";
                                        phandle = <0x36>;
                                };

                                soc-crit {
                                        temperature = <0x17318>;
                                        hysteresis = <0x7d0>;
                                        type = "critical";
                                        phandle = <0x890x8a>;
                                };
                        };

                        cooling-maps {

                                map0 {
                                        trip = <0x36>;
                                        cooling-device = <0x09 0xffffffff 0xffffffff 0x0a 0xffffffff
0xffffffff 0x0b 0xffffffff 0xffffffff 0x0c 0xffffffff 0xffffffff>;
                                        contribution = <0x1000>;
                                };

                                map1 {
                                        trip = <0x36>;
                                        cooling-device = <0x37 0xffffffff 0xffffffff>;
                                        contribution = <0x1000>;
                                };
                        };
                };
        };
```

```
tsadc@ff250000 {
	compatible = "rockchip,rk3328-tsadc";
	reg = <0x00 0xff250000 0x00 0x100>;
	interrupts = <0x00 0x3a 0x04>;
	assigned-clocks = <0x02 0x24>;
	assigned-clock-rates = <0xc350>;
	clocks = <0x02 0x24 0x02 0xd5>;
	clock-names = "tsadc\0apb_pclk";
	pinctrl-names = "init\0default\0sleep";
	pinctrl-0 = <0x38>;
	pinctrl-1 = <0x39>;
	pinctrl-2 = <0x38>;
	resets = <0x02 0x42>;
	reset-names = "tsadc-apb";
	rockchip,grf = <0x3a>;
	rockchip,hw-tshut-temp = <0x186a0>;
	#thermal-sensor-cells = <0x01>;
	status = "okay";
	rockchip,hw-tshut-mode = <0x00>;
	rockchip,hw-tshut-polarity = <0x00>;
	phandle = <0x35>;
};

efuse@ff260000 {
	compatible = "rockchip,rk3328-efuse";
	reg = <0x00 0xff260000 0x00 0x50>;
	#address-cells = <0x01>;
	#size-cells = <0x01>;
	clocks = <0x02 0x3e>;
	clock-names = "pclk_efuse";
	rockchip,efuse-size = <0x20>;
	phandle = <0x8a0x8b>;

	id@7 {
		reg = <0x07 0x10>;
		phandle = <0x8b0x8c>;
	};

	cpu-leakage@17 {
		reg = <0x17 0x01>;
		phandle = <0x8c0x8d>;
	};

	logic-leakage@19 {
		reg = <0x19 0x01>;
		phandle = <0x8d0x8e>;
	};

	cpu-version@1a {
		reg = <0x1a 0x01>;
		bits = <0x03 0x03>;
		phandle = <0x4a>;
```

```
                };
        };

        adc@ff280000 {
                compatible = "rockchip,rk3328-saradc\0rockchip,rk3399-saradc";
                reg = <0x00 0xff280000 0x00 0x100>;
                interrupts = <0x00 0x50 0x04>;
                #io-channel-cells = <0x01>;
                clocks = <0x02 0x25 0x02 0xea>;
                clock-names = "saradc\0apb_pclk";
                resets = <0x02 0x56>;
                reset-names = "saradc-apb";
                status = "disabled";
                phandle = <0x8e0x8f>;
        };

        gpu@ff300000 {
                compatible = "rockchip,rk3328-mali\0arm,mali-450";
                reg = <0x00 0xff300000 0x00 0x30000>;
                interrupts = <0x00 0x5a 0x04 0x00 0x57 0x04 0x00 0x5d 0x04 0x00 0x58 0x04
0x00 0x59 0x04 0x00 0x5b 0x04 0x00 0x5c 0x04>;
                interrupt-names = "gp\0gpmmu\0pp\0pp0\0ppmmu0\0pp1\0ppmmu1";
                clocks = <0x02 0x87 0x02 0x87>;
                clock-names = "bus\0core";
                operating-points-v2 = <0x3b>;
                power-domains = <0x3c 0x01>;
                resets = <0x02 0x66>;
                #cooling-cells = <0x02>;
                mali-supply = <0x3d>;
                phandle = <0x37>;
        };

        gpu-opp-table {
                compatible = "operating-points-v2";
                phandle = <0x3b>;

                opp-200000000 {
                        opp-hz = <0x00 0xbebc200>;
                        opp-microvolt = <0x100590>;
                };

                opp-300000000 {
                        opp-hz = <0x00 0x11e1a300>;
                        opp-microvolt = <0x100590>;
                };

                opp-400000000 {
                        opp-hz = <0x00 0x17d78400>;
                        opp-microvolt = <0x100590>;
                };

                opp-500000000 {
```

```
                opp-hz = <0x00 0x1dcd6500>;
                opp-microvolt = <0x118c30>;
                status = "disabled";
        };
};

iommu@ff330200 {
        compatible = "rockchip,iommu";
        reg = <0x00 0xff330200 0x00 0x100>;
        interrupts = <0x00 0x60 0x04>;
        interrupt-names = "h265e_mmu";
        clocks = <0x02 0x93 0x02 0xdd>;
        clock-names = "aclk\0iface";
        #iommu-cells = <0x00>;
        status = "disabled";
        phandle = <0x8f0x90>;
};

iommu@ff340800 {
        compatible = "rockchip,iommu";
        reg = <0x00 0xff340800 0x00 0x40>;
        interrupts = <0x00 0x62 0x04>;
        interrupt-names = "vepu_mmu";
        clocks = <0x02 0x8f 0x02 0x146>;
        clock-names = "aclk\0iface";
        #iommu-cells = <0x00>;
        status = "disabled";
        phandle = <0x900x91>;
};

video-codec@ff350000 {
        compatible = "rockchip,rk3328-vpu";
        reg = <0x00 0xff350000 0x00 0x800>;
        interrupts = <0x00 0x09 0x04>;
        interrupt-names = "vdpu";
        clocks = <0x02 0x8f 0x02 0x146>;
        clock-names = "aclk\0hclk";
        iommus = <0x3e>;
        power-domains = <0x3c 0x08>;
        phandle = <0x910x92>;
};

iommu@ff350800 {
        compatible = "rockchip,iommu";
        reg = <0x00 0xff350800 0x00 0x40>;
        interrupts = <0x00 0x0b 0x04>;
        interrupt-names = "vpu_mmu";
        clocks = <0x02 0x8f 0x02 0x146>;
        clock-names = "aclk\0iface";
        #iommu-cells = <0x00>;
        power-domains = <0x3c 0x08>;
        phandle = <0x3e>;
```

```
};

video-codec@ff360000 {
	compatible = "rockchip,rk3328-vdec\0rockchip,rk3399-vdec";
	reg = <0x00 0xff360000 0x00 0x480>;
	interrupts = <0x00 0x07 0x04>;
	interrupt-names = "vdpu";
	assigned-clocks = <0x02 0x8b 0x02 0x41 0x02 0x42>;
	assigned-clock-rates = <0x17d78400 0x17d78400 0x11e1a300>;
	clocks = <0x02 0x8b 0x02 0x142 0x02 0x41 0x02 0x42>;
	clock-names = "axi\0ahb\0cabac\0core";
	iommus = <0x3f>;
	power-domains = <0x3c 0x05>;
	resets = <0x02 0xa6 0x02 0xa4 0x02 0xa8 0x02 0xa9 0x02 0xa5 0x02 0xa7>;
	reset-names = "video_h\0video_a\0video_core\0video_cabac\0niu_a\0niu_h";
	phandle = <0x920x93>;
};

iommu@ff360480 {
	compatible = "rockchip,iommu";
	reg = <0x00 0xff360480 0x00 0x40 0x00 0xff3604c0 0x00 0x40>;
	interrupts = <0x00 0x4a 0x04>;
	interrupt-names = "rkvdec_mmu";
	clocks = <0x02 0x8b 0x02 0x142>;
	clock-names = "aclk\0iface";
	#iommu-cells = <0x00>;
	power-domains = <0x3c 0x05>;
	phandle = <0x3f>;
};

vop@ff370000 {
	compatible = "rockchip,rk3328-vop";
	reg = <0x00 0xff370000 0x00 0x3efc>;
	interrupts = <0x00 0x20 0x04>;
	clocks = <0x02 0x91 0x02 0x78 0x02 0x13b>;
	clock-names = "aclk_vop\0dclk_vop\0hclk_vop";
	resets = <0x02 0x85 0x02 0x86 0x02 0x87>;
	reset-names = "axi\0ahb\0dclk";
	iommus = <0x40>;
	status = "okay";
	phandle = <0x930x94>;

	port {
		#address-cells = <0x01>;
		#size-cells = <0x00>;
		phandle = <0x0d>;

		endpoint@0 {
			reg = <0x00>;
			remote-endpoint = <0x41>;
			phandle = <0x47>;
		};
```

```
		};
	};

	iommu@ff373f00 {
		compatible = "rockchip,iommu";
		reg = <0x00 0xff373f00 0x00 0x100>;
		interrupts = <0x00 0x20 0x04>;
		interrupt-names = "vop_mmu";
		clocks = <0x02 0x91 0x02 0x13b>;
		clock-names = "aclk\0iface";
		#iommu-cells = <0x00>;
		status = "okay";
		phandle = <0x40>;
	};

	iep@ff3a0000 {
		compatible = "rockchip,rk3328-iep\0rockchip,rk3228-iep";
		reg = <0x00 0xff3a0000 0x00 0x800>;
		interrupts = <0x00 0x1f 0x04>;
		interrupt-names = "iep";
		clocks = <0x02 0x9b 0x02 0x153>;
		clock-names = "axi\0ahb";
		power-domains = <0x3c 0x05>;
		iommus = <0x42>;
		phandle = <0x940x95>;
	};

	iommu@ff3a0800 {
		compatible = "rockchip,iommu";
		reg = <0x00 0xff3a0800 0x00 0x40>;
		interrupts = <0x00 0x1f 0x04>;
		interrupt-names = "iep_mmu";
		clocks = <0x02 0x9b 0x02 0x153>;
		clock-names = "aclk\0iface";
		power-domains = <0x3c 0x05>;
		#iommu-cells = <0x00>;
		phandle = <0x42>;
	};

	hdmi@ff3c0000 {
		compatible = "rockchip,rk3328-dw-hdmi";
		reg = <0x00 0xff3c0000 0x00 0x20000>;
		reg-io-width = <0x04>;
		interrupts = <0x00 0x23 0x04 0x00 0x47 0x04>;
		clocks = <0x02 0xe7 0x02 0x46 0x02 0x1e>;
		clock-names = "iahb\0isfr\0cec";
		phys = <0x43>;
		phy-names = "hdmi";
		pinctrl-names = "default";
		pinctrl-0 = <0x44 0x45 0x46>;
		rockchip,grf = <0x3a>;
		#sound-dai-cells = <0x00>;
```

```
                status = "okay";
                phandle = <0x0f>;

                ports {

                        port {
                                phandle = <0x950x96>;

                                endpoint {
                                        remote-endpoint = <0x47>;
                                        phandle = <0x41>;
                                };
                        };
                };
        };

        codec@ff410000 {
                compatible = "rockchip,rk3328-codec";
                reg = <0x00 0xff410000 0x00 0x1000>;
                clocks = <0x02 0xeb 0x02 0x2a>;
                clock-names = "pclk\0mclk";
                rockchip,grf = <0x3a>;
                #sound-dai-cells = <0x00>;
                status = "okay";
                mute-gpios = <0x48 0x00 0x01>;
                phandle = <0x08>;
        };

        phy@ff430000 {
                compatible = "rockchip,rk3328-hdmi-phy";
                reg = <0x00 0xff430000 0x00 0x10000>;
                interrupts = <0x00 0x53 0x04>;
                clocks = <0x02 0xe4 0x49 0x02 0x79>;
                clock-names = "sysclk\0refoclk\0refpclk";
                clock-output-names = "hdmi_phy";
                #clock-cells = <0x00>;
                nvmem-cells = <0x4a>;
                nvmem-cell-names = "cpu-version";
                #phy-cells = <0x00>;
                status = "okay";
                phandle = <0x43>;
        };

        clock-controller@ff440000 {
                compatible = "rockchip,rk3328-cru\0rockchip,cru\0syscon";
                reg = <0x00 0xff440000 0x00 0x1000>;
                rockchip,grf = <0x3a>;
                #clock-cells = <0x01>;
                #reset-cells = <0x01>;
                assigned-clocks = <0x02 0x78 0x02 0x3d 0x02 0x1e 0x02 0x26 0x02 0x27 0x02
0x28 0x02 0x88 0x02 0x89 0x02 0x8e 0x02 0x85 0x02 0x83 0x02 0x8a 0x02 0x8c 0x02 0x8d 0x02
```

```
0x41 0x02 0x42 0x02 0x44 0x02 0x43 0x02 0x22 0x02 0x5c 0x02 0x35 0x02 0x06 0x02 0x04
0x02 0x03 0x02 0x88 0x02 0x148 0x02 0xd8 0x02 0x89 0x02 0x134 0x02 0xe6 0x02 0x1e>;
                assigned-clock-parents = <0x02 0x7a 0x02 0x01 0x02 0x04 0x49 0x49 0x49>;
                assigned-clock-rates = <0x00 0x3a98000 0x00 0x16e3600 0x16e3600 0x16e3600
0xe4e1c0 0xe4e1c0 0x11e1a300 0x5f5e100 0x17d78400 0x5f5e100 0x2faf080 0x5f5e100
0x5f5e100 0x5f5e100 0x2faf080 0x2faf080 0x2faf080 0x2faf080 0x16e3600 0x23c34600
0x1d4c0000 0x47868c00 0x8f0d180 0x47868c0 0x47868c0 0x8f0d180 0x47868c0 0x47868c0
0x8000>;
                phandle = <0x02>;
        };

        syscon@ff450000 {
                compatible = "rockchip,rk3328-usb2phy-grf\0syscon\0simple-mfd";
                reg = <0x00 0xff450000 0x00 0x10000>;
                #address-cells = <0x01>;
                #size-cells = <0x01>;
                phandle = <0x960x97>;

                usb2phyusb2-phy@100 {
                        compatible = "rockchip,rk3328-usb2phy";
                        reg = <0x100 0x10>;
                        clocks = <0x49>;
                        clock-names = "phyclk";
                        clock-output-names = "usb480m_phy";
                        #clock-cells = <0x00>;
                        assigned-clocks = <0x02 0x7b>;
                        assigned-clock-parents = <0x4b>;
                        status = "okay";
                        phandle = <0x4b>;

                        otg-port {
                                #phy-cells = <0x00>;
                                interrupts = <0x00 0x3b 0x04 0x00 0x3c 0x04 0x00 0x3d 0x04>;
                                interrupt-names = "otg-bvalid\0otg-id\0linestate";
                                status = "okay";
                                phandle = <0x59>;
                        };

                        host-port {
                                #phy-cells = <0x00>;
                                interrupts = <0x00 0x3e 0x04>;
                                interrupt-names = "linestate";
                                status = "okay";
                                phandle = <0x5a>;
                        };
                };
        };

        mmc@ff500000 {
                compatible = "rockchip,rk3328-dw-mshc\0rockchip,rk3288-dw-mshc";
                reg = <0x00 0xff500000 0x00 0x4000>;
                interrupts = <0x00 0x0c 0x04>;
```

```
                clocks = <0x02 0x13d 0x02 0x21 0x02 0x4a 0x02 0x4e>;
                clock-names = "biu\0ciu\0ciu-drive\0ciu-sample";
                fifo-depth = <0x100>;
                max-frequency = <0x8f0d180>;
                resets = <0x02 0x6d>;
                reset-names = "reset";
                status = "okay";
                bus-width = <0x04>;
                cap-mmc-highspeed;
                cap-sd-highspeed;
                disable-wp;
                pinctrl-names = "default";
                pinctrl-0 = <0x4c 0x4d 0x4e 0x4f>;
                vmmc-supply = <0x1c>;
                vqmmc-supply = <0x1c>;
                phandle = <0x970x98>;
        };

        mmc@ff510000 {
                compatible = "rockchip,rk3328-dw-mshc\0rockchip,rk3288-dw-mshc";
                reg = <0x00 0xff510000 0x00 0x4000>;
                interrupts = <0x00 0x0d 0x04>;
                clocks = <0x02 0x13e 0x02 0x22 0x02 0x4b 0x02 0x4f>;
                clock-names = "biu\0ciu\0ciu-drive\0ciu-sample";
                fifo-depth = <0x100>;
                max-frequency = <0x8f0d180>;
                resets = <0x02 0x6e>;
                reset-names = "reset";
                status = "disabled";
                phandle = <0x980x99>;
        };

        mmc@ff520000 {
                compatible = "rockchip,rk3328-dw-mshc\0rockchip,rk3288-dw-mshc";
                reg = <0x00 0xff520000 0x00 0x4000>;
                interrupts = <0x00 0x0e 0x04>;
                clocks = <0x02 0x13f 0x02 0x23 0x02 0x4c 0x02 0x50>;
                clock-names = "biu\0ciu\0ciu-drive\0ciu-sample";
                fifo-depth = <0x100>;
                max-frequency = <0x8f0d180>;
                resets = <0x02 0x6f>;
                reset-names = "reset";
                status = "okay";
                bus-width = <0x08>;
                cap-mmc-highspeed;
                mmc-ddr-1_8v;
                mmc-hs200-1_8v;
                no-sd;
                no-sdio;
                non-removable;
                pinctrl-names = "default";
                pinctrl-0 = <0x50 0x51 0x52>;
```

```
                vmmc-supply = <0x1c>;
                vqmmc-supply = <0x1d>;
                phandle = <0x990x9a>;
        };

        ethernet@ff540000 {
                compatible = "rockchip,rk3328-gmac";
                reg = <0x00 0xff540000 0x00 0x10000>;
                interrupts = <0x00 0x18 0x04>;
                interrupt-names = "macirq";
                clocks = <0x02 0x64 0x02 0x57 0x02 0x58 0x02 0x5a 0x02 0x59 0x02 0x96 0x02
0xdf>;
                clock-names = "stmmaceth\0mac_clk_rx\0mac_clk_tx\0clk_mac_ref\
0clk_mac_refout\0aclk_mac\0pclk_mac";
                resets = <0x02 0x63>;
                reset-names = "stmmaceth";
                rockchip,grf = <0x3a>;
                snps,txpbl = <0x04>;
                status = "okay";
                assigned-clocks = <0x02 0x64 0x02 0x66>;
                assigned-clock-parents = <0x53 0x53>;
                clock_in_out = "input";
                phy-handle = <0x54>;
                phy-mode = "rgmii";
                phy-supply = <0x1c>;
                pinctrl-names = "default";
                pinctrl-0 = <0x55>;
                snps,aal;
                snps,pbl = <0x04>;
                tx_delay = <0x26>;
                rx_delay = <0x11>;
                phandle = <0x9a0x9b>;

                mdio {
                        compatible = "snps,dwmac-mdio";
                        #address-cells = <0x01>;
                        #size-cells = <0x00>;

                        ethernet-phy@0 {
                                reg = <0x00>;
                                reset-assert-us = <0x2710>;
                                reset-deassert-us = <0x7530>;
                                reset-gpios = <0x28 0x11 0x01>;
                                phandle = <0x54>;
                        };
                };
        };

        ethernet@ff550000 {
                compatible = "rockchip,rk3328-gmac";
                reg = <0x00 0xff550000 0x00 0x10000>;
                rockchip,grf = <0x3a>;
```

```
                interrupts = <0x00 0x15 0x04>;
                interrupt-names = "macirq";
                clocks = <0x02 0x54 0x02 0x53 0x02 0x53 0x02 0x55 0x02 0x95 0x02 0xde 0x02
0x56>;
                clock-names = "stmmaceth\0mac_clk_rx\0mac_clk_tx\0clk_mac_ref\0aclk_mac\
0pclk_mac\0clk_macphy";
                resets = <0x02 0x62 0x02 0x64>;
                reset-names = "stmmaceth\0mac-phy";
                phy-mode = "rmii";
                phy-handle = <0x56>;
                snps,txpbl = <0x04>;
                clock_in_out = "output";
                status = "okay";
                assigned-clock-rate = <0x2faf080>;
                assigned-clocks = <0x02 0x65>;
                assigned-clock-parents = <0x02 0x54>;
                phandle = <0x9b0x9c>;

                mdio {
                        compatible = "snps,dwmac-mdio";
                        #address-cells = <0x01>;
                        #size-cells = <0x00>;

                        ethernet-phy@0 {
                                compatible = "ethernet-phy-id1234.d400\0ethernet-phy-ieee802.3-
c22";

                                reg = <0x00>;
                                clocks = <0x02 0x56>;
                                resets = <0x02 0x64>;
                                pinctrl-names = "default";
                                pinctrl-0 = <0x57 0x58>;
                                phy-is-integrated;
                                phandle = <0x56>;
                        };
                };
        };

        usb@ff580000 {
                compatible = "rockchip,rk3328-usb\0rockchip,rk3066-usb\0snps,dwc2";
                reg = <0x00 0xff580000 0x00 0x40000>;
                interrupts = <0x00 0x17 0x04>;
                clocks = <0x02 0x14d>;
                clock-names = "otg";
                dr_mode = "host";
                g-np-tx-fifo-size = <0x10>;
                g-rx-fifo-size = <0x118>;
                g-tx-fifo-size = <0x100 0x80 0x80 0x40 0x20 0x10>;
                phys = <0x59>;
                phy-names = "usb2-phy";
                status = "okay";
                phandle = <0x9c0x9d>;
        };
```

```
        usb@ff5c0000 {
                compatible = "generic-ehci";
                reg = <0x00 0xff5c0000 0x00 0x10000>;
                interrupts = <0x00 0x10 0x04>;
                clocks = <0x02 0x14e 0x4b>;
                phys = <0x5a>;
                phy-names = "usb";
                status = "okay";
                pinctrl-names = "default";
                pinctrl-0 = <0x5b 0x5c 0x5d 0x5e 0x5f 0x60>;
                phandle = <0x9d0x9e>;
        };

        usb@ff5d0000 {
                compatible = "generic-ohci";
                reg = <0x00 0xff5d0000 0x00 0x10000>;
                interrupts = <0x00 0x11 0x04>;
                clocks = <0x02 0x14e 0x4b>;
                phys = <0x5a>;
                phy-names = "usb";
                status = "disabled";
                phandle = <0x9e>;
        };

        mmc@ff5f0000 {
                compatible = "rockchip,rk3328-dw-mshc\0rockchip,rk3288-dw-mshc";
                reg = <0x00 0xff5f0000 0x00 0x4000>;
                interrupts = <0x00 0x04 0x04>;
                clocks = <0x02 0x140 0x02 0x1f 0x02 0x4d 0x02 0x51>;
                clock-names = "biu\0ciu\0ciu-drive\0ciu-sample";
                fifo-depth = <0x100>;
                max-frequency = <0x8f0d180>;
                resets = <0x02 0x68>;
                reset-names = "reset";
                status = "disabled";
                phandle = <0x9f>;
        };

        usb@ff600000 {
                compatible = "rockchip,rk3328-dwc3\0snps,dwc3";
                reg = <0x00 0xff600000 0x00 0x100000>;
                interrupts = <0x00 0x43 0x04>;
                clocks = <0x02 0x60 0x02 0x61 0x02 0x84>;
                clock-names = "ref_clk\0suspend_clk\0bus_clk";
                dr_mode = "hostotg";
                phy_type = "utmi_wide";
                snps,dis-del-phy-power-chg-quirk;
                snps,dis_enblslpm_quirk;
                snps,dis-tx-ipgap-linecheck-quirk;
                snps,dis-u2-freeclk-exists-quirk;
                snps,dis_u2_susphy_quirk;
```

```
                snps,dis_u3_susphy_quirk;
                status = "okaydisabled";
                phandle = <0xa0>;
        };

        dwmmc@ff5f0000 {
                compatible = "rockchip,rk3328-dw-mshc\0rockchip,rk3288-dw-mshc";
                reg = <0x00 0xff5f0000 0x00 0x4000>;
                interrupts = <0x00 0x04 0x04>;
                clocks = <0x02 0x140 0x02 0x1f 0x02 0x4d 0x02 0x51>;
                clock-names = "biu\0ciu\0ciu-drive\0ciu-sample";
                fifo-depth = <0x100>;
                max-frequency = <0x8f0d180>;
                resets = <0x02 0x68>;
                reset-names = "reset";
                status = "disabled";
                phandle = <0xa1>;
        };

        interrupt-controller@ff811000 {
                compatible = "arm,gic-400";
                #interrupt-cells = <0x03>;
                #address-cells = <0x00>;
                interrupt-controller;
                reg = <0x00 0xff811000 0x00 0x1000 0x00 0xff812000 0x00 0x2000 0x00
0xff814000 0x00 0x2000 0x00 0xff816000 0x00 0x2000>;
                interrupts = <0x01 0x09 0xf04>;
                phandle = <0x01>;
        };

        pinctrl {
                compatible = "rockchip,rk3328-pinctrl";
                rockchip,grf = <0x3a>;
                #address-cells = <0x02>;
                #size-cells = <0x02>;
                ranges;
                phandle = <0xa10xa2>;

                gpiogpio0@ff210000 {
                        compatible = "rockchip,gpio-bank";
                        reg = <0x00 0xff210000 0x00 0x100>;
                        interrupts = <0x00 0x33 0x04>;
                        clocks = <0x02 0xc8>;
                        gpio-controller;
                        #gpio-cells = <0x02>;
                        interrupt-controller;
                        #interrupt-cells = <0x02>;
                        phandle = <0x6e>;
                };

                gpiogpio1@ff220000 {
                        compatible = "rockchip,gpio-bank";
```

```
                reg = <0x00 0xff220000 0x00 0x100>;
                interrupts = <0x00 0x34 0x04>;
                clocks = <0x02 0xc9>;
                gpio-controller;
                #gpio-cells = <0x02>;
                interrupt-controller;
                #interrupt-cells = <0x02>;
                phandle = <0xa20xa3>;
        };

        gpiogpio2@ff230000 {
                compatible = "rockchip,gpio-bank";
                reg = <0x00 0xff230000 0x00 0x100>;
                interrupts = <0x00 0x35 0x04>;
                clocks = <0x02 0xca>;
                gpio-controller;
                #gpio-cells = <0x02>;
                interrupt-controller;
                #interrupt-cells = <0x02>;
                phandle = <0x28>;
        };

        gpiogpio3@ff240000 {
                compatible = "rockchip,gpio-bank";
                reg = <0x00 0xff240000 0x00 0x100>;
                interrupts = <0x00 0x36 0x04>;
                clocks = <0x02 0xcb>;
                gpio-controller;
                #gpio-cells = <0x02>;
                interrupt-controller;
                #interrupt-cells = <0x02>;
                phandle = <0xa30xa4>;
        };

        pcfg-pull-up {
                bias-pull-up;
                phandle = <0x63>;
        };

        pcfg-pull-down {
                bias-pull-down;
                phandle = <0x6b>;
        };

        pcfg-pull-none {
                bias-disable;
                phandle = <0x61>;
        };

        pcfg-pull-none-2ma {
                bias-disable;
                drive-strength = <0x02>;
```

```
                phandle = <0x6a>;
        };

        pcfg-pull-up-2ma {
                bias-pull-up;
                drive-strength = <0x02>;
                phandle = <0xa40xa5>;
        };

        pcfg-pull-up-4ma {
                bias-pull-up;
                drive-strength = <0x04>;
                phandle = <0x64>;
        };

        pcfg-pull-none-4ma {
                bias-disable;
                drive-strength = <0x04>;
                phandle = <0x67>;
        };

        pcfg-pull-down-4ma {
                bias-pull-down;
                drive-strength = <0x04>;
                phandle = <0xa50xa6>;
        };

        pcfg-pull-none-8ma {
                bias-disable;
                drive-strength = <0x08>;
                phandle = <0x65>;
        };

        pcfg-pull-up-8ma {
                bias-pull-up;
                drive-strength = <0x08>;
                phandle = <0x66>;
        };

        pcfg-pull-none-12ma {
                bias-disable;
                drive-strength = <0x0c>;
                phandle = <0x68>;
        };

        pcfg-pull-up-12ma {
                bias-pull-up;
                drive-strength = <0x0c>;
                phandle = <0x69>;
        };

        pcfg-output-high {
```

```
        output-high;
        phandle = <0x6d>;
};

pcfg-output-low {
        output-low;
        phandle = <0x6c>;
};

pcfg-input-high {
        bias-pull-up;
        input-enable;
        phandle = <0x62>;
};

pcfg-input {
        input-enable;
        phandle = <0xa60xa7>;
};

i2c0 {

        i2c0-xfer {
                rockchip,pins = <0x02 0x18 0x01 0x61 0x02 0x19 0x01 0x61>;
                phandle = <0x26>;
        };
};

i2c1 {

        i2c1-xfer {
                rockchip,pins = <0x02 0x04 0x02 0x61 0x02 0x05 0x02 0x61>;
                phandle = <0x27>;
        };
};

i2c2 {

        i2c2-xfer {
                rockchip,pins = <0x02 0x0d 0x01 0x61 0x02 0x0e 0x01 0x61>;
                phandle = <0x2b>;
        };
};

i2c3 {

        i2c3-xfer {
                rockchip,pins = <0x00 0x05 0x02 0x61 0x00 0x06 0x02 0x61>;
                phandle = <0x2c>;
        };

        i2c3-pins {
```

```
                rockchip,pins = <0x00 0x05 0x00 0x61 0x00 0x06 0x00 0x61>;
                phandle = <0xa70xa8>;
        };
};

hdmi_i2c {

        hdmii2c-xfer {
                rockchip,pins = <0x00 0x05 0x01 0x61 0x00 0x06 0x01 0x61>;
                phandle = <0x45>;
        };
};

pdm-0 {

        pdmm0-clk {
                rockchip,pins = <0x02 0x12 0x02 0x61>;
                phandle = <0x12>;
        };

        pdmm0-fsync {
                rockchip,pins = <0x02 0x17 0x02 0x61>;
                phandle = <0xa80xa9>;
        };

        pdmm0-sdi0 {
                rockchip,pins = <0x02 0x13 0x02 0x61>;
                phandle = <0x13>;
        };

        pdmm0-sdi1 {
                rockchip,pins = <0x02 0x14 0x02 0x61>;
                phandle = <0x14>;
        };

        pdmm0-sdi2 {
                rockchip,pins = <0x02 0x15 0x02 0x61>;
                phandle = <0x15>;
        };

        pdmm0-sdi3 {
                rockchip,pins = <0x02 0x16 0x02 0x61>;
                phandle = <0x16>;
        };

        pdmm0-clk-sleep {
                rockchip,pins = <0x02 0x12 0x00 0x62>;
                phandle = <0x17>;
        };

        pdmm0-sdi0-sleep {
                rockchip,pins = <0x02 0x13 0x00 0x62>;
```

```
                phandle = <0x18>;
        };

        pdmm0-sdi1-sleep {
                rockchip,pins = <0x02 0x14 0x00 0x62>;
                phandle = <0x19>;
        };

        pdmm0-sdi2-sleep {
                rockchip,pins = <0x02 0x15 0x00 0x62>;
                phandle = <0x1a>;
        };

        pdmm0-sdi3-sleep {
                rockchip,pins = <0x02 0x16 0x00 0x62>;
                phandle = <0x1b>;
        };

        pdmm0-fsync-sleep {
                rockchip,pins = <0x02 0x17 0x00 0x62>;
                phandle = <0xa90xaa>;
        };
};

tsadc {

        otp-pin {
                rockchip,pins = <0x02 0x0d 0x00 0x61>;
                phandle = <0x38>;
        };

        otp-out {
                rockchip,pins = <0x02 0x0d 0x01 0x61>;
                phandle = <0x39>;
        };
};

uart0 {

        uart0-xfer {
                rockchip,pins = <0x01 0x09 0x01 0x61 0x01 0x08 0x01 0x63>;
                phandle = <0x1f>;
        };

        uart0-cts {
                rockchip,pins = <0x01 0x0b 0x01 0x61>;
                phandle = <0x20>;
        };

        uart0-rts {
                rockchip,pins = <0x01 0x0a 0x01 0x61>;
                phandle = <0x21>;
```

```
        };

        uart0-rts-pin {
                rockchip,pins = <0x01 0x0a 0x00 0x61>;
                phandle = <0xaa0xab>;
        };
};

uart1 {

        uart1-xfer {
                rockchip,pins = <0x03 0x04 0x04 0x61 0x03 0x06 0x04 0x63>;
                phandle = <0x22>;
        };

        uart1-cts {
                rockchip,pins = <0x03 0x07 0x04 0x61>;
                phandle = <0x23>;
        };

        uart1-rts {
                rockchip,pins = <0x03 0x05 0x04 0x61>;
                phandle = <0x24>;
        };

        uart1-rts-pin {
                rockchip,pins = <0x03 0x05 0x00 0x61>;
                phandle = <0xab0xac>;
        };
};

uart2-0 {

        uart2m0-xfer {
                rockchip,pins = <0x01 0x00 0x02 0x61 0x01 0x01 0x02 0x63>;
                phandle = <0xac0xad>;
        };
};

uart2-1 {

        uart2m1-xfer {
                rockchip,pins = <0x02 0x00 0x01 0x61 0x02 0x01 0x01 0x63>;
                phandle = <0x25>;
        };
};

spi0-0 {

        spi0m0-clk {
                rockchip,pins = <0x02 0x08 0x01 0x63>;
                phandle = <0xad0xae>;
```

```
        };

        spi0m0-cs0 {
                rockchip,pins = <0x02 0x0b 0x01 0x63>;
                phandle = <0xae0xaf>;
        };

        spi0m0-tx {
                rockchip,pins = <0x02 0x09 0x01 0x63>;
                phandle = <0xaf0xb0>;
        };

        spi0m0-rx {
                rockchip,pins = <0x02 0x0a 0x01 0x63>;
                phandle = <0xb00xb1>;
        };

        spi0m0-cs1 {
                rockchip,pins = <0x02 0x0c 0x01 0x63>;
                phandle = <0xb10xb2>;
        };
};

spi0-1 {

        spi0m1-clk {
                rockchip,pins = <0x03 0x17 0x02 0x63>;
                phandle = <0xb20xb3>;
        };

        spi0m1-cs0 {
                rockchip,pins = <0x03 0x1a 0x02 0x63>;
                phandle = <0xb30xb4>;
        };

        spi0m1-tx {
                rockchip,pins = <0x03 0x19 0x02 0x63>;
                phandle = <0xb40xb5>;
        };

        spi0m1-rx {
                rockchip,pins = <0x03 0x18 0x02 0x63>;
                phandle = <0xb50xb6>;
        };

        spi0m1-cs1 {
                rockchip,pins = <0x03 0x1b 0x02 0x63>;
                phandle = <0xb60xb7>;
        };
};

spi0-2 {
```

```
                spi0m2-clk {
                        rockchip,pins = <0x03 0x00 0x04 0x63>;
                        phandle = <0x2d>;
                };

                spi0m2-cs0 {
                        rockchip,pins = <0x03 0x08 0x03 0x63>;
                        phandle = <0x30>;
                };

                spi0m2-tx {
                        rockchip,pins = <0x03 0x01 0x04 0x63>;
                        phandle = <0x2e>;
                };

                spi0m2-rx {
                        rockchip,pins = <0x03 0x02 0x04 0x63>;
                        phandle = <0x2f>;
                };
        };

        i2s1 {

                i2s1-mclk {
                        rockchip,pins = <0x02 0x0f 0x01 0x61>;
                        phandle = <0xb70xb8>;
                };

                i2s1-sclk {
                        rockchip,pins = <0x02 0x12 0x01 0x61>;
                        phandle = <0xb80xb9>;
                };

                i2s1-lrckrx {
                        rockchip,pins = <0x02 0x10 0x01 0x61>;
                        phandle = <0xb90xba>;
                };

                i2s1-lrcktx {
                        rockchip,pins = <0x02 0x11 0x01 0x61>;
                        phandle = <0xba0xbb>;
                };

                i2s1-sdi {
                        rockchip,pins = <0x02 0x13 0x01 0x61>;
                        phandle = <0xbb0xbc>;
                };

                i2s1-sdo {
                        rockchip,pins = <0x02 0x17 0x01 0x61>;
                        phandle = <0xbc0xbd>;
```

```
                };

                i2s1-sdio1 {
                        rockchip,pins = <0x02 0x14 0x01 0x61>;
                        phandle = <0xbd0xbe>;
                };

                i2s1-sdio2 {
                        rockchip,pins = <0x02 0x15 0x01 0x61>;
                        phandle = <0xbe0xbf>;
                };

                i2s1-sdio3 {
                        rockchip,pins = <0x02 0x16 0x01 0x61>;
                        phandle = <0xbf0xc0>;
                };

                i2s1-sleep {
                        rockchip,pins = <0x02 0x0f 0x00 0x62 0x02 0x10 0x00 0x62 0x02
0x11 0x00 0x62 0x02 0x12 0x00 0x62 0x02 0x13 0x00 0x62 0x02 0x14 0x00 0x62 0x02 0x15
0x00 0x62 0x02 0x16 0x00 0x62 0x02 0x17 0x00 0x62>;
                        phandle = <0xc00xc1>;
                };
        };

        i2s2-0 {

                i2s2m0-mclk {
                        rockchip,pins = <0x01 0x15 0x01 0x61>;
                        phandle = <0xc10xc2>;
                };

                i2s2m0-sclk {
                        rockchip,pins = <0x01 0x16 0x01 0x61>;
                        phandle = <0xc20xc3>;
                };

                i2s2m0-lrckrx {
                        rockchip,pins = <0x01 0x1a 0x01 0x61>;
                        phandle = <0xc30xc4>;
                };

                i2s2m0-lrcktx {
                        rockchip,pins = <0x01 0x17 0x01 0x61>;
                        phandle = <0xc40xc5>;
                };

                i2s2m0-sdi {
                        rockchip,pins = <0x01 0x18 0x01 0x61>;
                        phandle = <0xc50xc6>;
                };
```

```
                        i2s2m0-sdo {
                                rockchip,pins = <0x01 0x19 0x01 0x61>;
                                phandle = <0xc60xc7>;
                        };

                        i2s2m0-sleep {
                                rockchip,pins = <0x01 0x15 0x00 0x62 0x01 0x16 0x00 0x62 0x01
0x1a 0x00 0x62 0x01 0x17 0x00 0x62 0x01 0x18 0x00 0x62 0x01 0x19 0x00 0x62>;
                                phandle = <0xc70xc8>;
                        };
                };

                i2s2-1 {

                        i2s2m1-mclk {
                                rockchip,pins = <0x01 0x15 0x01 0x61>;
                                phandle = <0xc80xc9>;
                        };

                        i2s2m1-sclk {
                                rockchip,pins = <0x03 0x00 0x06 0x61>;
                                phandle = <0xc90xca>;
                        };

                        i2sm1-lrckrx {
                                rockchip,pins = <0x03 0x08 0x06 0x61>;
                                phandle = <0xca0xcb>;
                        };

                        i2s2m1-lrcktx {
                                rockchip,pins = <0x03 0x08 0x04 0x61>;
                                phandle = <0xcb0xcc>;
                        };

                        i2s2m1-sdi {
                                rockchip,pins = <0x03 0x02 0x06 0x61>;
                                phandle = <0xcc0xcd>;
                        };

                        i2s2m1-sdo {
                                rockchip,pins = <0x03 0x01 0x06 0x61>;
                                phandle = <0xcd0xce>;
                        };

                        i2s2m1-sleep {
                                rockchip,pins = <0x01 0x15 0x00 0x62 0x03 0x00 0x00 0x62 0x03
0x08 0x00 0x62 0x03 0x02 0x00 0x62 0x03 0x01 0x00 0x62>;
                                phandle = <0xce0xcf>;
                        };
                };

                spdif-0 {
```

```
        spdifm0-tx {
                rockchip,pins = <0x00 0x1b 0x01 0x61>;
                phandle = <0x11>;
        };
};

spdif-1 {

        spdifm1-tx {
                rockchip,pins = <0x02 0x11 0x02 0x61>;
                phandle = <0xcf0xd0>;
        };
};

spdif-2 {

        spdifm2-tx {
                rockchip,pins = <0x00 0x02 0x02 0x61>;
                phandle = <0xd00xd1>;
        };
};

sdmmc0-0 {

        sdmmc0m0-pwren {
                rockchip,pins = <0x02 0x07 0x01 0x64>;
                phandle = <0xd10xd2>;
        };

        sdmmc0m0-pin {
                rockchip,pins = <0x02 0x07 0x00 0x64>;
                phandle = <0xd20xd3>;
        };
};

sdmmc0-1 {

        sdmmc0m1-pwren {
                rockchip,pins = <0x00 0x1e 0x03 0x64>;
                phandle = <0xd30xd4>;
        };

        sdmmc0m1-pin {
                rockchip,pins = <0x00 0x1e 0x00 0x64>;
                phandle = <0xd40xd5>;
        };
};

sdmmc0 {

        sdmmc0-clk {
```

```
                        rockchip,pins = <0x01 0x06 0x01 0x65>;
                        phandle = <0x4c>;
                };

                sdmmc0-cmd {
                        rockchip,pins = <0x01 0x04 0x01 0x66>;
                        phandle = <0x4d>;
                };

                sdmmc0-dectn {
                        rockchip,pins = <0x01 0x05 0x01 0x64>;
                        phandle = <0x4e>;
                };

                sdmmc0-wrprt {
                        rockchip,pins = <0x01 0x07 0x01 0x64>;
                        phandle = <0xd50xd6>;
                };

                sdmmc0-bus1 {
                        rockchip,pins = <0x01 0x00 0x01 0x66>;
                        phandle = <0xd60xd7>;
                };

                sdmmc0-bus4 {
                        rockchip,pins = <0x01 0x00 0x01 0x66 0x01 0x01 0x01 0x66 0x01
0x02 0x01 0x66 0x01 0x03 0x01 0x66>;
                        phandle = <0x4f>;
                };

                sdmmc0-pins {
                        rockchip,pins = <0x01 0x06 0x00 0x64 0x01 0x04 0x00 0x64 0x01
0x05 0x00 0x64 0x01 0x07 0x00 0x64 0x01 0x03 0x00 0x64 0x01 0x02 0x00 0x64 0x01 0x01
0x00 0x64 0x01 0x00 0x00 0x64>;
                        phandle = <0xd70xd8>;
                };
        };

        sdmmc0ext {

                sdmmc0ext-clk {
                        rockchip,pins = <0x03 0x02 0x03 0x67>;
                        phandle = <0xd80xd9>;
                };

                sdmmc0ext-cmd {
                        rockchip,pins = <0x03 0x00 0x03 0x64>;
                        phandle = <0xd90xda>;
                };

                sdmmc0ext-wrprt {
                        rockchip,pins = <0x03 0x03 0x03 0x64>;
```

```
                        phandle = <0xda0xdb>;
                    };

                    sdmmc0ext-dectn {
                        rockchip,pins = <0x03 0x01 0x03 0x64>;
                        phandle = <0xdb0xdc>;
                    };

                    sdmmc0ext-bus1 {
                        rockchip,pins = <0x03 0x04 0x03 0x64>;
                        phandle = <0xdc0xdd>;
                    };

                    sdmmc0ext-bus4 {
                        rockchip,pins = <0x03 0x04 0x03 0x64 0x03 0x05 0x03 0x64 0x03
0x06 0x03 0x64 0x03 0x07 0x03 0x64>;
                        phandle = <0xdd0xde>;
                    };

                    sdmmc0ext-pins {
                        rockchip,pins = <0x03 0x00 0x00 0x64 0x03 0x01 0x00 0x64 0x03
0x02 0x00 0x64 0x03 0x03 0x00 0x64 0x03 0x04 0x00 0x64 0x03 0x05 0x00 0x64 0x03 0x06
0x00 0x64 0x03 0x07 0x00 0x64>;
                        phandle = <0xde0xdf>;
                    };
                };

                sdmmc1 {

                    sdmmc1-clk {
                        rockchip,pins = <0x01 0x0c 0x01 0x65>;
                        phandle = <0xdf0xe0>;
                    };

                    sdmmc1-cmd {
                        rockchip,pins = <0x01 0x0d 0x01 0x66>;
                        phandle = <0xe00xe1>;
                    };

                    sdmmc1-pwren {
                        rockchip,pins = <0x01 0x12 0x01 0x66>;
                        phandle = <0xe10xe2>;
                    };

                    sdmmc1-wrprt {
                        rockchip,pins = <0x01 0x14 0x01 0x66>;
                        phandle = <0xe20xe3>;
                    };

                    sdmmc1-dectn {
                        rockchip,pins = <0x01 0x13 0x01 0x66>;
                        phandle = <0xe30xe4>;
```

```
                };

                sdmmc1-bus1 {
                        rockchip,pins = <0x01 0x0e 0x01 0x66>;
                        phandle = <0xe40xe5>;
                };

                sdmmc1-bus4 {
                        rockchip,pins = <0x01 0x0e 0x01 0x66 0x01 0x0f 0x01 0x66 0x01
0x10 0x01 0x66 0x01 0x11 0x01 0x66>;
                        phandle = <0xe50xe6>;
                };

                sdmmc1-pins {
                        rockchip,pins = <0x01 0x0c 0x00 0x64 0x01 0x0d 0x00 0x64 0x01
0x0e 0x00 0x64 0x01 0x0f 0x00 0x64 0x01 0x10 0x00 0x64 0x01 0x11 0x00 0x64 0x01 0x12 0x00
0x64 0x01 0x13 0x00 0x64 0x01 0x14 0x00 0x64>;
                        phandle = <0xe60xe7>;
                };
        };

        emmc {

                emmc-clk {
                        rockchip,pins = <0x03 0x15 0x02 0x68>;
                        phandle = <0x50>;
                };

                emmc-cmd {
                        rockchip,pins = <0x03 0x13 0x02 0x69>;
                        phandle = <0x51>;
                };

                emmc-pwren {
                        rockchip,pins = <0x03 0x16 0x02 0x61>;
                        phandle = <0xe70xe8>;
                };

                emmc-rstnout {
                        rockchip,pins = <0x03 0x14 0x02 0x61>;
                        phandle = <0xe80xe9>;
                };

                emmc-bus1 {
                        rockchip,pins = <0x00 0x07 0x02 0x69>;
                        phandle = <0xe90xea>;
                };

                emmc-bus4 {
                        rockchip,pins = <0x00 0x07 0x02 0x69 0x02 0x1c 0x02 0x69 0x02
0x1d 0x02 0x69 0x02 0x1e 0x02 0x69>;
                        phandle = <0xea0xeb>;
```

```
                };

                emmc-bus8 {
                        rockchip,pins = <0x00 0x07 0x02 0x69 0x02 0x1c 0x02 0x69 0x02
0x1d 0x02 0x69 0x02 0x1e 0x02 0x69 0x02 0x1f 0x02 0x69 0x03 0x10 0x02 0x69 0x03 0x11 0x02
0x69 0x03 0x12 0x02 0x69>;
                        phandle = <0x52>;
                };
        };

        pwm0 {

                pwm0-pin {
                        rockchip,pins = <0x02 0x04 0x01 0x61>;
                        phandle = <0x31>;
                };
        };

        pwm1 {

                pwm1-pin {
                        rockchip,pins = <0x02 0x05 0x01 0x61>;
                        phandle = <0x32>;
                };
        };

        pwm2 {

                pwm2-pin {
                        rockchip,pins = <0x02 0x06 0x01 0x61>;
                        phandle = <0x33>;
                };
        };

        pwmir {

                pwmir-pin {
                        rockchip,pins = <0x02 0x02 0x01 0x61>;
                        phandle = <0x34>;
                };
        };

        gmac-1 {

                rgmiim1-pins {
                        rockchip,pins = <0x01 0x0c 0x02 0x65 0x01 0x0d 0x02 0x67 0x01
0x13 0x02 0x67 0x01 0x19 0x02 0x65 0x01 0x15 0x02 0x67 0x01 0x16 0x02 0x67 0x01 0x17
0x02 0x67 0x01 0x0a 0x02 0x67 0x01 0x0b 0x02 0x67 0x01 0x08 0x02 0x65 0x01 0x09 0x02
0x65 0x01 0x0e 0x02 0x67 0x01 0x0f 0x02 0x67 0x01 0x10 0x02 0x65 0x01 0x11 0x02 0x65 0x00
0x08 0x01 0x65 0x00 0x0c 0x01 0x65 0x00 0x18 0x01 0x67 0x00 0x10 0x01 0x65 0x00 0x11 0x01
0x65 0x00 0x17 0x01 0x65 0x00 0x16 0x01 0x65>;
                        phandle = <0x55>;
```

```
                };

                rmiim1-pins {
                        rockchip,pins = <0x01 0x13 0x02 0x6a 0x01 0x19 0x02 0x68 0x01
0x15 0x02 0x6a 0x01 0x18 0x02 0x6a 0x01 0x16 0x02 0x6a 0x01 0x17 0x02 0x6a 0x01 0x0a 0x02
0x6a 0x01 0x0b 0x02 0x6a 0x01 0x08 0x02 0x68 0x01 0x09 0x02 0x68 0x00 0x0b 0x01 0x61 0x00
0x0c 0x01 0x61 0x00 0x18 0x01 0x61 0x00 0x13 0x01 0x61 0x00 0x10 0x01 0x61 0x00 0x11 0x01
0x61>;
                        phandle = <0xeb0xec>;
                };
        };

        gmac2phy {

                fephyled-speed10 {
                        rockchip,pins = <0x00 0x1e 0x01 0x61>;
                        phandle = <0xec0xed>;
                };

                fephyled-duplex {
                        rockchip,pins = <0x00 0x1e 0x02 0x61>;
                        phandle = <0xed0xee>;
                };

                fephyled-rxm1 {
                        rockchip,pins = <0x02 0x19 0x02 0x61>;
                        phandle = <0x57>;
                };

                fephyled-txm1 {
                        rockchip,pins = <0x02 0x19 0x03 0x61>;
                        phandle = <0xee0xef>;
                };

                fephyled-linkm1 {
                        rockchip,pins = <0x02 0x18 0x02 0x61>;
                        phandle = <0x58>;
                };
        };

        tsadc_pin {

                tsadc-int {
                        rockchip,pins = <0x02 0x0d 0x02 0x61>;
                        phandle = <0xef0xf0>;
                };

                tsadc-pin {
                        rockchip,pins = <0x02 0x0d 0x00 0x61>;
                        phandle = <0xf00xf1>;
                };
        };
```

```
		hdmi_pin {

			hdmi-cec {
				rockchip,pins = <0x00 0x03 0x01 0x61>;
				phandle = <0x44>;
			};

			hdmi-hpd {
				rockchip,pins = <0x00 0x04 0x01 0x6b>;
				phandle = <0x46>;
			};
		};

		cif-0 {

			dvp-d2d9-m0 {
				rockchip,pins = <0x03 0x04 0x02 0x61 0x03 0x05 0x02 0x61 0x03
0x06 0x02 0x61 0x03 0x07 0x02 0x61 0x03 0x08 0x02 0x61 0x03 0x09 0x02 0x61 0x03 0x0a
0x02 0x61 0x03 0x0b 0x02 0x61 0x03 0x01 0x02 0x61 0x03 0x00 0x02 0x61 0x03 0x03 0x02
0x61 0x03 0x02 0x02 0x61>;
				phandle = <0xf10xf2>;
			};
		};

		cif-1 {

			dvp-d2d9-m1 {
				rockchip,pins = <0x03 0x04 0x02 0x61 0x03 0x05 0x02 0x61 0x03
0x06 0x02 0x61 0x03 0x07 0x02 0x61 0x03 0x08 0x02 0x61 0x02 0x10 0x04 0x61 0x02 0x11
0x04 0x61 0x02 0x12 0x04 0x61 0x03 0x01 0x02 0x61 0x03 0x00 0x02 0x61 0x02 0x0f 0x04 0x61
0x03 0x02 0x02 0x61>;
				phandle = <0xf20xf3>;
			};
		};

		pmic {

			pmic-int-l {
				rockchip,pins = <0x02 0x06 0x00 0x63>;
				phandle = <0x29>;
			};
		};

		usb3 {

			usb30-host-drv {
				rockchip,pins = <0x00 0x00 0x00 0x61>;
				phandle = <0x6f>;
			};
		};
```

```
		wifi {

			bt-dis {
				rockchip,pins = <0x02 0x15 0x00 0x6c>;
				phandle = <0x5b>;
			};

			bt-wake-host {
				rockchip,pins = <0x02 0x10 0x00 0x63>;
				phandle = <0x5c>;
			};

			chip-en {
				rockchip,pins = <0x02 0x13 0x00 0x6c>;
				phandle = <0x5d>;
			};

			host-wake-bt {
				rockchip,pins = <0x02 0x0f 0x00 0x6d>;
				phandle = <0x5e>;
			};

			wl-dis {
				rockchip,pins = <0x03 0x08 0x00 0x6c>;
				phandle = <0x5f>;
			};

			wl-wake-host {
				rockchip,pins = <0x03 0x01 0x00 0x63>;
				phandle = <0x60>;
			};
		};
};

chosen {
		stdout-path = "serial2:1500000n8";
};

external-gmac-clock {
		compatible = "fixed-clock";
		clock-frequency = <0x7735940>;
		clock-output-names = "gmac_clkin";
		#clock-cells = <0x00>;
		phandle = <0x53>;
};

usb3-current-switch {
		compatible = "regulator-fixed";
		enable-active-high;
		gpio = <0x6e 0x00 0x00>;
		pinctrl-names = "default";
		pinctrl-0 = <0x6f>;
```

```
		regulator-name = "vcc_host_5v";
		vin-supply = <0x2a>;
		phandle = <0xf30xf4>;
	};

	vcc-sys {
		compatible = "regulator-fixed";
		regulator-name = "vcc_sys";
		regulator-min-microvolt = <0x4c4b40>;
		regulator-max-microvolt = <0x4c4b40>;
		phandle = <0x2a>;
	};

	ir-receiver {
		compatible = "gpio-ir-receiver";
		gpios = <0x28 0x02 0x01>;
		linux,rc-map-name = "rc-beelink-gs1";
	};

	spdif-sound {
		compatible = "simple-audio-card";
		simple-audio-card,name = "SPDIF";
		phandle = <0xf40xf5>;

		simple-audio-card,cpu {
			sound-dai = <0x70>;
		};

		simple-audio-card,codec {
			sound-dai = <0x71>;
		};
	};

	spdif-dit {
		compatible = "linux,spdif-dit";
		#sound-dai-cells = <0x00>;
		phandle = <0x71>;
	};

	__symbols__ {
		cpu0 = "/cpus/cpu@0";
		cpu1 = "/cpus/cpu@1";
		cpu2 = "/cpus/cpu@2";
		cpu3 = "/cpus/cpu@3";
		CPU_SLEEP = "/cpus/idle-states/cpu-sleep";
		l2 = "/cpus/l2-cache0";
		cpu0_opp_table = "/opp-table-0-table0";
		amba = "/bus";
		dmac = "/bus/dmac@ff1f0000";
		analog_sound = "/analog-sound";
		display_subsystem = "/display-subsystem";
		hdmi_sound = "/hdmi-sound";
```

```
xin24m = "/xin24m";
i2s0 = "/i2s@ff000000";
i2s1 = "/i2s@ff010000";
i2s2 = "/i2s@ff020000";
spdif = "/spdif@ff030000";
pdm = "/pdm@ff040000";
grf = "/syscon@ff100000";
io_domains = "/syscon@ff100000/io-domains";
grf_gpio = "/syscon@ff100000/grf-gpio";
power = "/syscon@ff100000/power-controller";
uart0 = "/serial@ff110000";
uart1 = "/serial@ff120000";
uart2 = "/serial@ff130000";
i2c0 = "/i2c@ff150000";
i2c1 = "/i2c@ff160000";
vdd_logic = "/i2c@ff160000/pmic@18/regulators/DCDC_REG1";
vdd_arm = "/i2c@ff160000/pmic@18/regulators/DCDC_REG2";
vcc_ddr = "/i2c@ff160000/pmic@18/regulators/DCDC_REG3";
vcc_io = "/i2c@ff160000/pmic@18/regulators/DCDC_REG4";
vdd_18 = "/i2c@ff160000/pmic@18/regulators/LDO_REG1";
vcc18_emmc = "/i2c@ff160000/pmic@18/regulators/LDO_REG2";
vdd_11 = "/i2c@ff160000/pmic@18/regulators/LDO_REG3";
i2c2 = "/i2c@ff170000";
i2c3 = "/i2c@ff180000";
spi0 = "/spi@ff190000";
wdt = "/watchdog@ff1a0000";
pwm0 = "/pwm@ff1b0000";
pwm1 = "/pwm@ff1b0010";
pwm2 = "/pwm@ff1b0020";
pwm3 = "/pwm@ff1b0030";
dmac = "/dma-controller@ff1f0000";
soc_thermal = "/thermal-zones/soc-thermal";
threshold = "/thermal-zones/soc-thermal/trips/trip-point0";
target = "/thermal-zones/soc-thermal/trips/trip-point1";
soc_crit = "/thermal-zones/soc-thermal/trips/soc-crit";
tsadc = "/tsadc@ff250000";
efuse = "/efuse@ff260000";
efuse_id = "/efuse@ff260000/id@7";
cpu_leakage = "/efuse@ff260000/cpu-leakage@17";
logic_leakage = "/efuse@ff260000/logic-leakage@19";
efuse_cpu_version = "/efuse@ff260000/cpu-version@1a";
saradc = "/adc@ff280000";
gpu = "/gpu@ff300000";
gpu_opp_table = "/gpu-opp-table";
h265e_mmu = "/iommu@ff330200";
vepu_mmu = "/iommu@ff340800";
vpu = "/video-codec@ff350000";
vpu_mmu = "/iommu@ff350800";
rkvdec = "/video-codec@ff360000";
rkvdec_mmu = "/iommu@ff360480";
vop = "/vop@ff370000";
vop_out = "/vop@ff370000/port";
```

```
vop_out_hdmi = "/vop@ff370000/port/endpoint@0";
vop_mmu = "/iommu@ff373f00";
iep = "/iep@ff3a0000";
iep_mmu = "/iommu@ff3a0800";
hdmi = "/hdmi@ff3c0000";
hdmi_in = "/hdmi@ff3c0000/ports/port";
hdmi_in_vop = "/hdmi@ff3c0000/ports/port/endpoint";
codec = "/codec@ff410000";
hdmiphy = "/phy@ff430000";
cru = "/clock-controller@ff440000";
usb2phy_grf = "/syscon@ff450000";
u2phy = "/syscon@ff450000/usb2phyusb2-phy@100";
u2phy_otg = "/syscon@ff450000/usb2phyusb2-phy@100/otg-port";
u2phy_host = "/syscon@ff450000/usb2phyusb2-phy@100/host-port";
sdmmc = "/mmc@ff500000";
sdio = "/mmc@ff510000";
emmc = "/mmc@ff520000";
gmac2io = "/ethernet@ff540000";
rtl8211f = "/ethernet@ff540000/mdio/ethernet-phy@0";
gmac2phy = "/ethernet@ff550000";
phy = "/ethernet@ff550000/mdio/ethernet-phy@0";
usb20_otg = "/usb@ff580000";
usb_host0_ehci = "/usb@ff5c0000";
usb_host0_ohci = "/usb@ff5d0000";
sdmmc_ext = "/mmc@ff5f0000";
usbdrd3 = "/usb@ff600000";
sdmmc_ext = "/dwmmc@ff5f0000";
gic = "/interrupt-controller@ff811000";
pinctrl = "/pinctrl";
gpio0 = "/pinctrl/gpiogpio0@ff210000";
gpio1 = "/pinctrl/gpiogpio1@ff220000";
gpio2 = "/pinctrl/gpiogpio2@ff230000";
gpio3 = "/pinctrl/gpiogpio3@ff240000";
pcfg_pull_up = "/pinctrl/pcfg-pull-up";
pcfg_pull_down = "/pinctrl/pcfg-pull-down";
pcfg_pull_none = "/pinctrl/pcfg-pull-none";
pcfg_pull_none_2ma = "/pinctrl/pcfg-pull-none-2ma";
pcfg_pull_up_2ma = "/pinctrl/pcfg-pull-up-2ma";
pcfg_pull_up_4ma = "/pinctrl/pcfg-pull-up-4ma";
pcfg_pull_none_4ma = "/pinctrl/pcfg-pull-none-4ma";
pcfg_pull_down_4ma = "/pinctrl/pcfg-pull-down-4ma";
pcfg_pull_none_8ma = "/pinctrl/pcfg-pull-none-8ma";
pcfg_pull_up_8ma = "/pinctrl/pcfg-pull-up-8ma";
pcfg_pull_none_12ma = "/pinctrl/pcfg-pull-none-12ma";
pcfg_pull_up_12ma = "/pinctrl/pcfg-pull-up-12ma";
pcfg_output_high = "/pinctrl/pcfg-output-high";
pcfg_output_low = "/pinctrl/pcfg-output-low";
pcfg_input_high = "/pinctrl/pcfg-input-high";
pcfg_input = "/pinctrl/pcfg-input";
i2c0_xfer = "/pinctrl/i2c0/i2c0-xfer";
i2c1_xfer = "/pinctrl/i2c1/i2c1-xfer";
i2c2_xfer = "/pinctrl/i2c2/i2c2-xfer";
```

```
i2c3_xfer = "/pinctrl/i2c3/i2c3-xfer";
i2c3_pins = "/pinctrl/i2c3/i2c3-pins";
hdmii2c_xfer = "/pinctrl/hdmi_i2c/hdmii2c-xfer";
pdmm0_clk = "/pinctrl/pdm-0/pdmm0-clk";
pdmm0_fsync = "/pinctrl/pdm-0/pdmm0-fsync";
pdmm0_sdi0 = "/pinctrl/pdm-0/pdmm0-sdi0";
pdmm0_sdi1 = "/pinctrl/pdm-0/pdmm0-sdi1";
pdmm0_sdi2 = "/pinctrl/pdm-0/pdmm0-sdi2";
pdmm0_sdi3 = "/pinctrl/pdm-0/pdmm0-sdi3";
pdmm0_clk_sleep = "/pinctrl/pdm-0/pdmm0-clk-sleep";
pdmm0_sdi0_sleep = "/pinctrl/pdm-0/pdmm0-sdi0-sleep";
pdmm0_sdi1_sleep = "/pinctrl/pdm-0/pdmm0-sdi1-sleep";
pdmm0_sdi2_sleep = "/pinctrl/pdm-0/pdmm0-sdi2-sleep";
pdmm0_sdi3_sleep = "/pinctrl/pdm-0/pdmm0-sdi3-sleep";
pdmm0_fsync_sleep = "/pinctrl/pdm-0/pdmm0-fsync-sleep";
otp_pin = "/pinctrl/tsadc/otp-pin";
otp_out = "/pinctrl/tsadc/otp-out";
uart0_xfer = "/pinctrl/uart0/uart0-xfer";
uart0_cts = "/pinctrl/uart0/uart0-cts";
uart0_rts = "/pinctrl/uart0/uart0-rts";
uart0_rts_pin = "/pinctrl/uart0/uart0-rts-pin";
uart1_xfer = "/pinctrl/uart1/uart1-xfer";
uart1_cts = "/pinctrl/uart1/uart1-cts";
uart1_rts = "/pinctrl/uart1/uart1-rts";
uart1_rts_pin = "/pinctrl/uart1/uart1-rts-pin";
uart2m0_xfer = "/pinctrl/uart2-0/uart2m0-xfer";
uart2m1_xfer = "/pinctrl/uart2-1/uart2m1-xfer";
spi0m0_clk = "/pinctrl/spi0-0/spi0m0-clk";
spi0m0_cs0 = "/pinctrl/spi0-0/spi0m0-cs0";
spi0m0_tx = "/pinctrl/spi0-0/spi0m0-tx";
spi0m0_rx = "/pinctrl/spi0-0/spi0m0-rx";
spi0m0_cs1 = "/pinctrl/spi0-0/spi0m0-cs1";
spi0m1_clk = "/pinctrl/spi0-1/spi0m1-clk";
spi0m1_cs0 = "/pinctrl/spi0-1/spi0m1-cs0";
spi0m1_tx = "/pinctrl/spi0-1/spi0m1-tx";
spi0m1_rx = "/pinctrl/spi0-1/spi0m1-rx";
spi0m1_cs1 = "/pinctrl/spi0-1/spi0m1-cs1";
spi0m2_clk = "/pinctrl/spi0-2/spi0m2-clk";
spi0m2_cs0 = "/pinctrl/spi0-2/spi0m2-cs0";
spi0m2_tx = "/pinctrl/spi0-2/spi0m2-tx";
spi0m2_rx = "/pinctrl/spi0-2/spi0m2-rx";
i2s1_mclk = "/pinctrl/i2s1/i2s1-mclk";
i2s1_sclk = "/pinctrl/i2s1/i2s1-sclk";
i2s1_lrckrx = "/pinctrl/i2s1/i2s1-lrckrx";
i2s1_lrcktx = "/pinctrl/i2s1/i2s1-lrcktx";
i2s1_sdi = "/pinctrl/i2s1/i2s1-sdi";
i2s1_sdo = "/pinctrl/i2s1/i2s1-sdo";
i2s1_sdio1 = "/pinctrl/i2s1/i2s1-sdio1";
i2s1_sdio2 = "/pinctrl/i2s1/i2s1-sdio2";
i2s1_sdio3 = "/pinctrl/i2s1/i2s1-sdio3";
i2s1_sleep = "/pinctrl/i2s1/i2s1-sleep";
i2s2m0_mclk = "/pinctrl/i2s2-0/i2s2m0-mclk";
```

```
i2s2m0_sclk = "/pinctrl/i2s2-0/i2s2m0-sclk";
i2s2m0_lrckrx = "/pinctrl/i2s2-0/i2s2m0-lrckrx";
i2s2m0_lrcktx = "/pinctrl/i2s2-0/i2s2m0-lrcktx";
i2s2m0_sdi = "/pinctrl/i2s2-0/i2s2m0-sdi";
i2s2m0_sdo = "/pinctrl/i2s2-0/i2s2m0-sdo";
i2s2m0_sleep = "/pinctrl/i2s2-0/i2s2m0-sleep";
i2s2m1_mclk = "/pinctrl/i2s2-1/i2s2m1-mclk";
i2s2m1_sclk = "/pinctrl/i2s2-1/i2s2m1-sclk";
i2s2m1_lrckrx = "/pinctrl/i2s2-1/i2sm1-lrckrx";
i2s2m1_lrcktx = "/pinctrl/i2s2-1/i2s2m1-lrcktx";
i2s2m1_sdi = "/pinctrl/i2s2-1/i2s2m1-sdi";
i2s2m1_sdo = "/pinctrl/i2s2-1/i2s2m1-sdo";
i2s2m1_sleep = "/pinctrl/i2s2-1/i2s2m1-sleep";
spdifm0_tx = "/pinctrl/spdif-0/spdifm0-tx";
spdifm1_tx = "/pinctrl/spdif-1/spdifm1-tx";
spdifm2_tx = "/pinctrl/spdif-2/spdifm2-tx";
sdmmc0m0_pwren = "/pinctrl/sdmmc0-0/sdmmc0m0-pwren";
sdmmc0m0_pin = "/pinctrl/sdmmc0-0/sdmmc0m0-pin";
sdmmc0m1_pwren = "/pinctrl/sdmmc0-1/sdmmc0m1-pwren";
sdmmc0m1_pin = "/pinctrl/sdmmc0-1/sdmmc0m1-pin";
sdmmc0_clk = "/pinctrl/sdmmc0/sdmmc0-clk";
sdmmc0_cmd = "/pinctrl/sdmmc0/sdmmc0-cmd";
sdmmc0_dectn = "/pinctrl/sdmmc0/sdmmc0-dectn";
sdmmc0_wrprt = "/pinctrl/sdmmc0/sdmmc0-wrprt";
sdmmc0_bus1 = "/pinctrl/sdmmc0/sdmmc0-bus1";
sdmmc0_bus4 = "/pinctrl/sdmmc0/sdmmc0-bus4";
sdmmc0_pins = "/pinctrl/sdmmc0/sdmmc0-pins";
sdmmc0ext_clk = "/pinctrl/sdmmc0ext/sdmmc0ext-clk";
sdmmc0ext_cmd = "/pinctrl/sdmmc0ext/sdmmc0ext-cmd";
sdmmc0ext_wrprt = "/pinctrl/sdmmc0ext/sdmmc0ext-wrprt";
sdmmc0ext_dectn = "/pinctrl/sdmmc0ext/sdmmc0ext-dectn";
sdmmc0ext_bus1 = "/pinctrl/sdmmc0ext/sdmmc0ext-bus1";
sdmmc0ext_bus4 = "/pinctrl/sdmmc0ext/sdmmc0ext-bus4";
sdmmc0ext_pins = "/pinctrl/sdmmc0ext/sdmmc0ext-pins";
sdmmc1_clk = "/pinctrl/sdmmc1/sdmmc1-clk";
sdmmc1_cmd = "/pinctrl/sdmmc1/sdmmc1-cmd";
sdmmc1_pwren = "/pinctrl/sdmmc1/sdmmc1-pwren";
sdmmc1_wrprt = "/pinctrl/sdmmc1/sdmmc1-wrprt";
sdmmc1_dectn = "/pinctrl/sdmmc1/sdmmc1-dectn";
sdmmc1_bus1 = "/pinctrl/sdmmc1/sdmmc1-bus1";
sdmmc1_bus4 = "/pinctrl/sdmmc1/sdmmc1-bus4";
sdmmc1_pins = "/pinctrl/sdmmc1/sdmmc1-pins";
emmc_clk = "/pinctrl/emmc/emmc-clk";
emmc_cmd = "/pinctrl/emmc/emmc-cmd";
emmc_pwren = "/pinctrl/emmc/emmc-pwren";
emmc_rstnout = "/pinctrl/emmc/emmc-rstnout";
emmc_bus1 = "/pinctrl/emmc/emmc-bus1";
emmc_bus4 = "/pinctrl/emmc/emmc-bus4";
emmc_bus8 = "/pinctrl/emmc/emmc-bus8";
pwm0_pin = "/pinctrl/pwm0/pwm0-pin";
pwm1_pin = "/pinctrl/pwm1/pwm1-pin";
pwm2_pin = "/pinctrl/pwm2/pwm2-pin";
```

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                pwmir_pin = "/pinctrl/pwmir/pwmir-pin";
                rgmiim1_pins = "/pinctrl/gmac-1/rgmiim1-pins";
                rmiim1_pins = "/pinctrl/gmac-1/rmiim1-pins";
                fephyled_speed10 = "/pinctrl/gmac2phy/fephyled-speed10";
                fephyled_duplex = "/pinctrl/gmac2phy/fephyled-duplex";
                fephyled_rxm1 = "/pinctrl/gmac2phy/fephyled-rxm1";
                fephyled_txm1 = "/pinctrl/gmac2phy/fephyled-txm1";
                fephyled_linkm1 = "/pinctrl/gmac2phy/fephyled-linkm1";
                tsadc_int = "/pinctrl/tsadc_pin/tsadc-int";
                tsadc_pin = "/pinctrl/tsadc_pin/tsadc-pin";
                hdmi_cec = "/pinctrl/hdmi_pin/hdmi-cec";
                hdmi_hpd = "/pinctrl/hdmi_pin/hdmi-hpd";
                dvp_d2d9_m0 = "/pinctrl/cif-0/dvp-d2d9-m0";
                dvp_d2d9_m1 = "/pinctrl/cif-1/dvp-d2d9-m1";
                pmic_int_l = "/pinctrl/pmic/pmic-int-l";
                usb30_host_drv = "/pinctrl/usb3/usb30-host-drv";
                bt_dis = "/pinctrl/wifi/bt-dis";
                bt_wake_host = "/pinctrl/wifi/bt-wake-host";
                chip_en = "/pinctrl/wifi/chip-en";
                host_wake_bt = "/pinctrl/wifi/host-wake-bt";
                wl_dis = "/pinctrl/wifi/wl-dis";
                wl_wake_host = "/pinctrl/wifi/wl-wake-host";
                gmac_clkin = "/external-gmac-clock";
                vcc_host_5v = "/usb3-current-switch";
                vcc_sys = "/vcc-sys";
                spdif_sound = "/spdif-sound";
                spdif_dit = "/spdif-dit";
        };
};
                mmc0 = "/mmc@ff500000";
                mmc1 = "/mmc@ff510000";
                mmc2 = "/mmc@ff520000";
```